

WHAT IS CLAIMED IS:

1. For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit configured to generate a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

2. The balancing circuit as recited in Claim 1 wherein said first driver comprises a plurality of vertical PNP transistors.

3. The balancing circuit as recited in Claim 1 wherein said second driver comprises a plurality of vertical NPN transistors.

4. The balancing circuit as recited in Claim 1 wherein said sensing subcircuit comprises at least one diode-connected transistor configured to substantially replicate said current gain characteristic of said first driver.

5. The balancing circuit as recited in Claim 1 wherein said
2 compensation subcircuit comprises a current repeater.

6. The balancing circuit as recited in Claim 1 wherein said
2 compensation subcircuit comprises emitter coupled logic configured
3 to provide said current gain compensation signal.

7. The balancing circuit as recited in Claim 1 wherein said
2 first and second current gain characteristics comprise a ratio of
3 collector-to-base current of devices associated with said first and
4 second drivers.

8. For use with a circuit having first and second
2 complementary drivers exhibiting different current gain
3 characteristics, a method of operating a balancing circuit,
4 comprising:
5 providing a correction signal indicating a first current
6 gain characteristic of said first driver; and
7 generating a current gain compensation signal to said
8 first driver to substantially match a second current gain
9 characteristic of said second driver based on said correction
10 signal.

9. The method as recited in Claim 8 wherein said first
2 driver comprises a plurality of vertical PNP transistors.

10. The method as recited in Claim 8 wherein said second
2 driver comprises a plurality of vertical NPN transistors.

11. The method as recited in Claim 8 wherein said providing
2 is performed by a sensing subcircuit including at least one diode-
3 connected transistor that substantially replicates said current
4 gain characteristic of said first driver.

12. The method as recited in Claim 8 wherein said generating
2 is performed by a compensation subcircuit including a current
3 repeater.

13. The method as recited in Claim 8 wherein said generating
2 is performed by a compensation subcircuit including emitter coupled
3 logic that provides said current gain compensation signal.

14. The method as recited in Claim 8 wherein said first and
2 second current gain characteristics comprise a ratio of collector-
3 to-base current of devices associated with said first and second
4 drivers.

15. A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit,
that receives a signal associated with a charging signal and
provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal
proportional to a phase difference between said output signal
having said output frequency and an input reference signal having
an input frequency; and

a charge pump that provides said charging signal via first and
second complementary drivers exhibiting different current gain
characteristics, said charge pump employing a balancing circuit,
including:

a sensing subcircuit that provides a correction signal
indicating a first current gain characteristic of said first
driver; and

a compensation subcircuit that generates a current gain
compensation signal to said first driver to substantially
match a second current gain characteristic of said second
driver based on said correction signal.

16. The PLL circuit as recited in Claim 15 wherein said first
driver comprises a plurality of vertical PNP transistors.

17. The PLL circuit as recited in Claim 15 wherein said
2 second driver comprises a plurality of vertical NPN transistors.

18. The PLL circuit as recited in Claim 15 wherein said
2 sensing subcircuit comprises at least one diode-connected
3 transistor that substantially replicates said current gain
4 characteristic of said first driver.

19. The PLL circuit as recited in Claim 15 wherein said
2 compensation subcircuit comprises a current repeater.

20. The PLL circuit as recited in Claim 15 wherein said
2 compensation subcircuit comprises emitter coupled logic that
3 provides said current gain compensation signal.

21. The PLL circuit as recited in Claim 15 wherein said first
2 and second current gain characteristics comprise a ratio of
3 collector-to-base current of devices associated with said first and
4 second drivers.